REMARKS

Claims 1-25 have been canceled without prejudice or disclaimer. New claims 26-30 have been added. Accordingly, claims 26-30 are currently pending in the application.

Submitted herewith is a certified priority document (JP No. 2000-306048). Applicant requests the Examiner to acknowledge the safe receipt of this document.

The title of the invention has been amended into a more descriptive form as required by the Examiner. The specification and Abstract have been amended to cure minor grammatical and idiomatic informalities. No new matter has been added.

The rejection of the claims under 35 U.S.C. §112, 35 U.S.C. §102 (namely as being anticipated by Yamasaki et al) and 35 U.S.C. §103 (namely as being unpatentable over Yamasaki et al in view of either Ishigaki or Nawamaki et al) have been rendered moot in view of the cancellation of those claims without prejudice or disclaimer. It is submitted that new claims 26-30 satisfy the requirements of 35 U.S.C. §112 and patentably define the present invention over the cited references.

The present invention, as recited in claim 26, is directed to a method of manufacturing a semiconductor device

in which a flexible wiring substrate is provided having a plurality of device areas and a plurality of electrodes formed on each device area. Semiconductor chips are provided each having a main surface and a plurality of electrodes formed on this main surface. The semiconductor chips are respectively mounted on the device areas. Electrodes of the semiconductor chips are connected with electrodes of the flexible wiring substrate using conductive members. The semiconductor chips and the plural device areas are sealed by a resin body formed according to a block molding method. The flexible wiring substrate and the resin body are cut to divide them into respective device areas using a cutting blade. In this cutting step, a rotation axis of the cutting blade is positioned over the back surface of the flexible wiring substrate. The cutting blade is advanced so as to push the flexible wiring substrate against the resin body with a cutting edge thereof. None of the cited references whether taken individually or in combination, disclose these features of the present invention.

Yamasaki et al disclose a process of resin sealing a semiconductor device and a lead frame. The electrically insulating film includes a first group of aperture portions including aperture portions provided in regions outside the

lead formation regions and a second group of aperture portions consisting of a plurality of aperture portions provided in the lead formation regions (see Abstract).

The Examiner refers to the teachings of Ishigaki and Nawamaki et al for teaching cutting methods. However, these references disclose that down cutting is available to avoid chipping. A translation of the Ishigaki reference is enclosed. As disclosed by Ishigaki at paragraph [0003] of the translation, since the "influence of the chipping on the front face of a wafer etc. cannot come out of the down cutting method easily while the state of a cutting side becomes good compared with the delivering-uppercut method, the down cutting method is in use now." However, neither of these references disclose that there is a problem of chipping when cutting a flexible wiring substrate with a resin body using a dicing blade. Therefore, these references do not recognize that the down cutting method is available to avoid the chipping of the flexible wiring substrate when a flexible substrate base is arranged at a side that comes into contact with the dicing blade.

As stated in the present claims, the rotation axis of the cutting blade is positioned over the back surface of the flexible wiring substrate and the cutting blade is advanced

with its cutting edge so as to push the flexible wiring substrate against the resin body. It is submitted that the cited references do not provide the motivation necessary for arriving at Applicants' inventive claimed process of cutting a flexible wiring substrate with a resin body. As such, it is submitted that the pending claims patentably define the present invention over the cited art.

In view of the foregoing amendments and remarks, Applicant contends that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination are respectfully requested.

Respectfully submitted,

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Date: September 19, 2002

MARKED UP VERSION OF REPLACED PARAGRAPHS OF THE SPECIFICATION

Page 1, first and second full paragraphs (lines 2-11), the marked up paragraphs are as follows:

The present invention relates to a semiconductor manufacturing technique and more particularly to a technique useful in its application to the improvement in the quality of a semiconductor device.

As [an] examples of [a] semiconductor devices having a semiconductor chip with a semiconductor integrated circuit formed thereon, further having bump electrodes (e.g., solder balls) as external terminals and a wiring board which supports the semiconductor chip, there [is] are known CSPs (Chip Scale Packages) or BGAs (Ball Grid Arrays).

Pages 1 and 2, the paragraph bridging these pages from page 1, line 22 to page 2, line 6, the marked up paragraph is as follows:

According to the block molding method, [there is used] a multi device substrate is used on which plural device areas corresponding to thin film wiring boards are formed in a partitioned and contiguous manner and are sealed with resin by

molding while being covered together. After the sealing with resin, dicing is performed for division (formation of individual pieces) into each device area.

Page 2, first full paragraph (lines 7-11), the marked up paragraph is as follows:

This [As to a] semiconductor device manufacturing method using such a block molding method, as well as the structure of the semiconductor device[, they] are disclosed, for example, in Japanese Unexamined Patent Publication No. 2000-124163 or Hei 11(1999)-214588.

Page 2, third full paragraph (lines 19-25), the marked up paragraph is as follows:

As described in the above publication, the case where an internal stress is created due to a difference in thermal expansion coefficient between the substrate and the molding resin [premises] is based on the premise that the strength of the substrate is so high as to generate a force resistive to a relative deformation (difference in volume change) between the molding resin and the substrate.

Page 3, second full paragraph (lines 9-15), the marked up paragraph is as follows:

Thus, the molding resin and the substrate give rise to a relative deformation due to a difference in thermal expansion coefficient or shrinkage of the resin on curing[,]. However, [but] by adopting a substrate which is flexible enough to follow up the deformation of the molding resin, it is possible to keep the internal stress between the substrate and the molding resin very low.